AMENDMENTS TO THE CLAIMS

1-9. (Cancelled).

10. (Previously Presented) An apparatus comprising:

a first output to provide a precharge value during a precharge phase and a true carry generate value during an evaluation phase;

a second output to provide the precharge value during the precharge phase and the compliment of the true carry generate true during the evaluation phase;

a current input;

a first evaluation block connected to the current input and the second output and having a plurality of transistors, wherein a number of said transistors are connected in a parallel relationship and a number of said transistors are connected in a serial relationship, wherein the first evaluation block comprises a first transistor with a drain connected to the second output, a second transistor with a drain connected to the source of the first transistor and a source connected to the current input, a third transistor with a drain connected to the second output, a fourth transistor with a drain connected to the source of the third transistor and a source connected to the current input, and a fifth transistor with a drain connected to the second output and a source connected to the drain of the fourth transistor; and

a second evaluation block connected to the current input and the first output and having a plurality of transistors, wherein the second evaluation block has the same number of transistors connected in a parallel relationship as the first evaluation block and the same number of transistors connected in a serial relationship as the first evaluation block.

11. (Original) The apparatus of claim 10, wherein the output drive strength for the first output is the same as the output drive strength for the second output.

12. (Previously Presented) The apparatus of claim 10, wherein the circuit further comprises a clock input to receive a clock having precharge and evaluation phases.

13. (Previously Presented) The apparatus of claim 12, wherein the current input is a transistor having a source node connected to ground and a gate connected to the clock input.

14. (Original) The apparatus of claim 13, wherein the gate of each transistor in the first evaluation block is connected to one of a set of true inputs and the gate of each of the transistors in the second evaluation block is connected to one of a set of compliment inputs, and wherein the load for the true inputs is the same as the load for the compliment inputs.

15-19. (Cancelled).

20. (Previously Presented) An apparatus comprising:

a true sum to provide a precharge signal during the precharge phase and the result of a sum function during the evaluation phase;

a compliment sum output to provide the precharge signal during the precharge phase and the compliment of the true sum output during the evaluation phase;

a current input;

a first evaluation block connected to the current input, the true sum output, and the compliment sum output, wherein the first evaluation block has a plurality of transistors, and wherein a number of said transistors are connected in parallel and a number of said transistors are connected in serial, wherein the first transistor has a drain connected to the compliment sum output, the second transistor has a drain connected to the source of the first transistor and a source connected to the drain of the fifth transistor, the third transistor has a drain connected to the true sum output, the fourth transistor has a drain connected to the source of the third transistor and a source connected to the drain of the fifth transistor, and the fifth transistor has a source connected to the current input; and

a second evaluation block connected to the current input and the true sum output and having a plurality of transistors, wherein the second evaluation block has the same number of transistors connected in parallel as the first evaluation block and the same number of transistors connected in serial as the first evaluation block.

21. (Original) The apparatus of claim 20, wherein the output drive strength for the true sum output is the same as the output drive strength for the compliment sum output.

22. (Cancelled).

23. (Previously Presented) The apparatus of claim 20, wherein the gate of the first transistor is connected to an exclusive-OR input, the gate of the second transistor is connected to a first generate input, the gate of the third transistor is connected to a compliment exclusive-OR input,

the gate of the fourth transistor is connected to a second generate input, and the gate of the fifth transistor is connected to a propagate input.

24. (Original) The apparatus of claim 20, wherein the transistors in the first evaluation block and second evaluation block are N-channel metal-oxide semiconductor (NMOS) transistors.

25-31. (Cancelled).

32. (Previously Presented) An apparatus comprising:

a first output to provide a precharge value during a precharge phase and a true carry generate value during an evaluation phase;

a second output to provide the precharge value during the precharge phase and the compliment of the true carry generate true during the evaluation phase;

a current input;

a first evaluation block connected to the current input and the second output and having a plurality of transistors, wherein a number of said transistors are connected in a parallel relationship and a number of said transistors are connected in a serial relationship, wherein the first evaluation block comprises a first transistor with a drain connected to the second output, a second transistor with a drain connected to the source of the first transistor and a source connected to the current input, a third transistor with a drain connected to the second output, a fourth transistor with a drain connected to the source of the third transistor and a source

connected to the current input, and a fifth transistor with a drain connected to the second output and a source connected to the drain of the fourth transistor; and

a second evaluation block connected to the current input and the first output and having a plurality of transistors, wherein the second evaluation block has the same number of transistors connected in a parallel relationship as the first evaluation block and the same number of transistors connected in a serial relationship as the first evaluation block wherein the circuit further comprises a clock input to receive a clock having precharge and evaluation phases and further wherein the gates of the first transistor and third transistor are connected to a first of the true inputs, the gates of the second transistor and fifth transistor are connected to a second of the true inputs, and the gate of the fourth transistor is connected to a third of the true inputs.

33. (Currently Amended) The apparatus of ~~claim 16~~ claim 32, wherein the precharge block comprises a first precharge transistor connected to a second current input and a second precharge transistor connected to a third current input, and wherein the first and second precharge transistors each have a gate connected to the clock.

34. (Currently Amended) The apparatus of ~~claim 17~~ claim 33, wherein the apparatus further comprises a keeper connected to each of the first output, second output, first evaluation block, and second evaluation block.

35. (Currently Amended) The apparatus of ~~claim 18~~ claim 34, wherein the transistors in the first evaluation block and second evaluation block are N-channel metal-oxide semiconductor

(NMOS) transistors, wherein first and second precharge transistor are P-channel metal-oxide semiconductor (PMOS) transistors, and wherein the keeper comprises two PMOS transistors.